

# Built-In Self-Test Architectures

Proposed problems

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# Problem 1

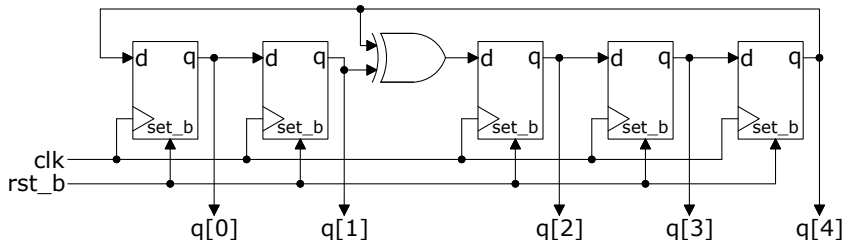
Design a D type flip-flop having asynchronous, active low, set and reset inputs. The asynchronous set input has higher priority compared to the reset input. The interface of the flip-flop is the following:

```
1 module d_ff (  
2     input clk ,      //clock input  
3     input rst_b ,   //reset input, clears flip-flop  
4     input set_b ,   //set input, sets flip-flop  
5     input d,        //synchronous data line  
6     output reg q    //flip-flop output  
7 );
```

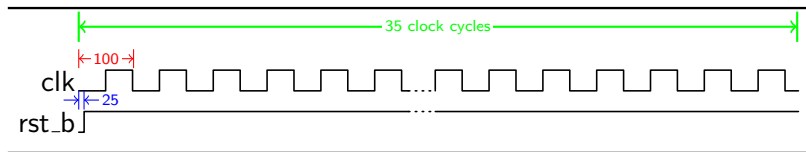
**Note:** no testbench is required

## Problem 2

Construct the architecture for module *lfsr5b* depicted below:

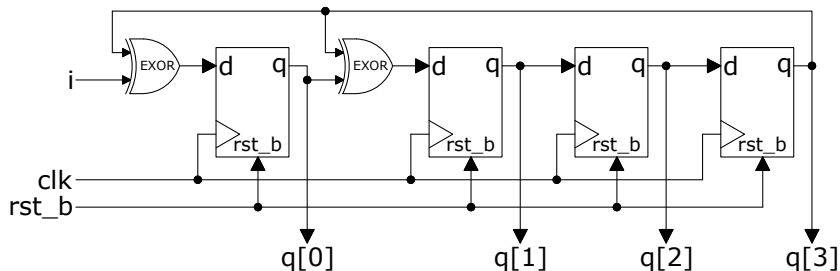


Determine the periodicity of output sequence using a testbench generating the inputs like in the timing diagram below:



## Problem 3

Construct the architecture for module *sisr4b* depicted below:



**Note:** no testbench is required

## Problem 4

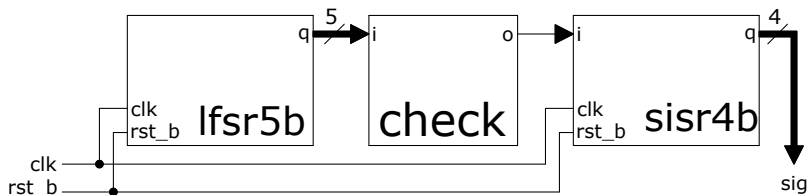
Build a module called *check* having one input *i* on 5 bits and one output *o* on 1 bit. The output is active if the unsigned number at the input is a multiple of 8. The module's interface is presented bellow:

```
1 module check (  
2     input [4:0] i ,  
3     output o  
4 );
```

**Note:** no testbench is required

## Problem 5

Construct the architecture for module *bist* depicted bellow:



Test the unit with a testbench generating the inputs like in the timing diagram bellow:

