Iterated addition

Proposed problems

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Problem 1

Starting from the architecture of a sequential multi-operand adder, build a structure for calculating the following sum:

$$\sum_{i=1}^{199}(3 * i - 2)$$

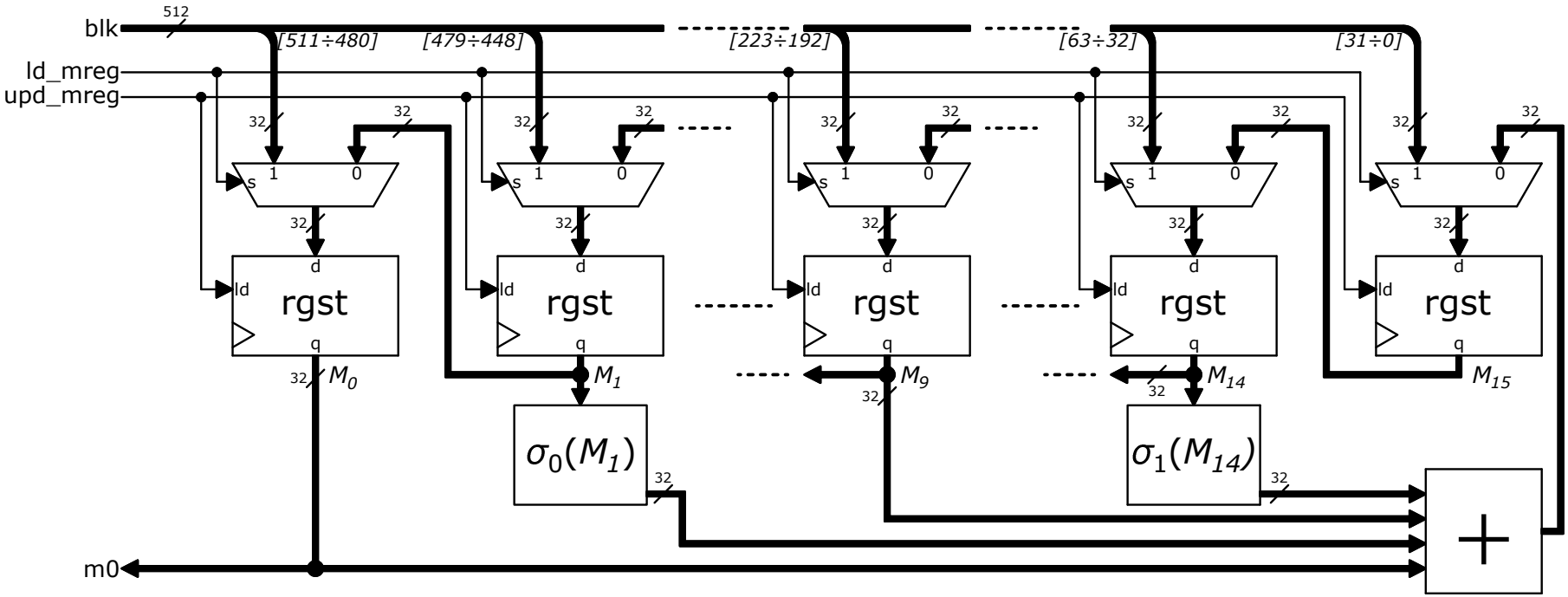
The module should be called, *mlopadd*, having inputs *clk*(1 bit), *rst_b*(1 bit), *x*(on the required number of bits that allows connecting to it all values $3 * i - 2, \forall\ 0 \leq i \leq 199$) and output *a*(on the required number of bits allowing for representing the above sum).

Your solution should include:

1. the script file, "run_mlopadd.txt"
2. a testbench generating the input signals in such a manner to facilitates computation of the above sum.

Problem 2

Build the datapath component responsible for the message schedule of a SHA-256 architecture, depicted bellow:



The unit, called, *mschdpath* has inputs *clk*(1 bit), *rst_b*(1 bit), *ld_mreg*(1 bit), *upd_mreg*(1 bit), *blk*(512 bits) and output *m0*(32 bits).

Problem 2 (contd.)

The multiplexors on registers' input should be implemented as Verilog functions, as well as the σ_0 and σ_1 operators used by the message scheduler's data path.

Your solution should include:

1. the Verilog code
2. the script file, "run_mschdpath.txt"
3. a testbench generating inputs as in the timing diagram bellow